Challenges

*Could 10-20% yields for Cell processors lead to problems for Sony PS3?*

- "With standard SiGe single-core processors, IBM can achieve yields of up to 95%. But with a chip like the Cell processor, you are lucky to get 10 or 20 percent."
- "If you really want to be focused on reliability and up-time availability, you can design one of these chips to self-detect. You can ship it with eight cores working, blow one of them, and from a user perspective you would have self-healed it in the field."
- "With such systems in place, yields could conceivably increase in a best-case scenario to 40% -- still significantly lower than the 95% yields that IBM and others enjoyed during the single-core, 'one-by-one' era."

Objectives

- Understanding impact of core yield, manufacturing and in-field test quality and spare scheme on the system yield and cost.
- How many spare cores should be included?
- How many working spares in a shipped chip would be sufficient?
- What is the requirement for manufacturing and in-field test quality to achieve required system reliability?
- Can we skip burn-in and repair infant mortality in the field?

Chip Cost Model

- Total cost: \( C_{\text{tot}} = C_{\text{man}} + C_{\text{ser}} \)
- Manufacturing cost: \( C_{\text{man}} = \alpha C_{\text{sys}} \)
- Service cost: \( C_{\text{ser}} = (1-\theta)C_{\text{sys}} \)

Burn-in Elimination

- With \( \alpha<3 \) and \( Y_{\text{sys}} \approx 90\% \) it is better not to do burn-in.
- With \( \alpha<2 \) and \( Y_{\text{sys}} \approx 95\% \) it is better not to do burn-in.

Summary & Future Works

- An analytical model for the cost of a spare-enhanced multi-core system, with or without burn-in.
- Reducing the overall cost by adding fewer spare cores.
- Investigating the removal of the burn-in process.
- Illustrating the importance of in-field test quality vs. the manufacturing test quality.

Future Works:

- Considering the communication infrastructure of an NoC-based SoC in the analysis:
  - Routers
  - Network Interfaces
  - Links
- Generalizing from homogeneity to heterogeneity:
  - Memory blocks, FPGA blocks, IP cores, DSPs, and et al.
- Applying the analysis to some available NoC-based SoCs:
  - Intel Itanium processor
  - IBM Power processor
  - University of Texas at Austin's TRIPS processor.